

Education News

Accurate Simulation Models Yield High-Efficiency Power Amplifier Design

■ **Sonoko Akamatsu, Charles Baylis, and Larry Dunleavy**

The design of RF and microwave power amplifiers continues to be somewhat of an art yet to be reduced to a systematic repeatable design practice on a wide-scale basis, despite the many excellent treatments of the subject in the literature (e.g., [1]) and a number of courses. The general unavailability of sufficiently accurate and reliable nonlinear models for power transistors has been a major factor in limiting the accuracy of power amplifier (PA) simulation results. Suitable nonlinear models must properly treat the nonlinear and combined dc/ac analysis required for proper power compression and efficiency simulation under varied load and bias conditions. In this article, an accurate nonlinear transistor model is shown to form the basis for a systematic simulation-based design procedure for a microwave PA. As an illustration of the procedure, a high-efficiency PA was developed with excellent first-pass performance results. This circuit was designed using a nonlinear transistor model and passive component models commercially available from University of South Florida (USF) spin-out company Modelithics, Inc. [2], [3] in combination with Agilent Technologies Advanced Design System software [4]. An 8-W PA with 62% efficiency was achieved at 1.3 GHz, without modification of the circuit. This circuit was awarded first place in an IEEE sponsored PA design competition. (See "Student High Efficiency PA Design Competition.")

Design Goals and a Simulation-Based Process for PA Design

The initial design goals for the PA are shown in Table 1. These goals are thought to be reasonable based on previously reported achievements in high-efficiency PA design. One push-pull amplifier design detailed in the literature has shown 60.9% power-added efficiency (PAE) at 4.15 GHz with an output power of 28.2 dBm [5], and another push-pull design has been reported to provide 63.8% PAE at 3.55 GHz and 28 dBm output power using harmonic tuning [6]. Such results show that achieving over 50% PAE for the targeted single-ended Class AB design should be a reasonable goal.

Table 1. Original design goals.

Frequency	1,489 MHz (1,477–1,501 MHz)
Bandwidth	>24 MHz
P1dB	38 dBm
Gain	14 dB
Pin	25 dBm max
PAE	Maximum (>50%)

For the design described in this article, a center frequency of 1,489 MHz

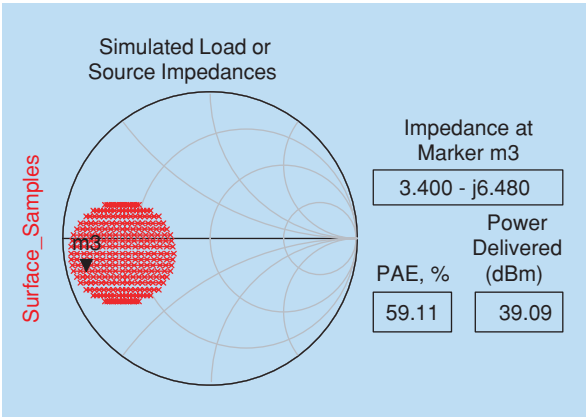


Figure 1. *Load-pull simulation in ADS with the input set to 1.7–j8.4 Ω. Input power is 25 dBm at 1.49 GHz. $V_{ds} = 10$ V, $V_{gs} = -2.0$ V.*

Sonoko Akamatsu, formerly with the University of South Florida, is with RF Micro Devices in Greensboro, North Carolina. Charles Baylis is with the University of South Florida in Tampa, Florida. Larry Dunleavy (Dunleavy@eng.usf.edu) is with the University of South Florida and Modelithics in Tampa, Florida.

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was targeted along with a 1-dB compression power (P_{1dB}) goal of 38 dBm output at 25 dBm input power (P_{in}). The goal was to achieve maximum PAE once the other minimum requirements had been met, and a PAE of over 50% was targeted for Class AB operation. A Fujitsu FLL120MK GaAs FET was selected to achieve these goals. According to its data sheet, this device is capable of 10 W at 2.3 GHz with greater than 40% efficiency [7].

Table 2 shows the systematic design process followed for the developed amplifier. The key to the success of the process was to have suitable models available for all the active and passive components and transmission line structures used. The transistor model provided by Modelithics for the FLL120MK was an EEHEMT model [4],

Student High Efficiency PA Design Competition

To promote student interest in microwave engineering, the Microwave Theory and Techniques High Power Microwave Components Committee (MTT-5) is sponsoring a new competition. Contestants are required to design and construct a microwave PA with the highest possible efficiency. The first competition took place at IMS 2005. Students and graduate students from all educational establishments were encouraged to enter. The PA had to operate at a frequency above 1 but less than 20 GHz, and have an output power level of at least 5 but less than 100 W into a 50-Ω load. The winning entry was the PA that demonstrated the highest PAE during testing at IMS 2005. The contest took place in the Interactive Forum (IF) area, and the results were on display during IF session hours. The winner received a prize of US$1,000 and was invited to submit a paper describing the design for the MTT *IEEE Microwave Magazine*.

The 2005 competition attracted entries from five universities (Ecole Polytechnique de Montréal; Sogang University, Korea; University of California, Davis; University of California, San Diego; and University of South Florida) plus a sixth demonstration only entry (Postech University, Korea). The PAs were fabricated and tested prior to the contest and carried to IMS 2005 by team members. The test equipment used to evaluate the PAs was provided by Agilent Technologies and centered about a PNA Vector Network Analyzer programmed to display PAE. Special thanks must be given to the Agilent volunteers headed by Ken Wong for their assistance with the measurements. Each team was given time to optimize their amplifiers for the best efficiency. Most of the PAs operated near the minimum frequency of 1 GHz, where high efficiency should most easily be achieved. The winning entry came from the University of South Florida and was designed by Sonoko Akamatsu, advised by Prof. Larry Dunleavy. It produced an efficiency of 61.7% and operated near 1.5 GHz. The highest measured efficiency of 69.2% was actually produced by Postech's PA, but it was not part of the official competition. The entry from Ecole Polytechnique de Montréal, which used a Doherty design and achieved a PAE 50.4%, is also worthy of note; its unique design allowed this efficiency to be produced at a higher power backoff with higher linearity than the other entries. The PA entry from the University of California, San Diego, achieved a PAE of 58.85%. The Postech's HPA had exemplary performance also, but was not part of the official competition.

Supervision and judging of the contest were provided by Steve Cripps, Jim Komiak, and Allen Katz from the MTT-5 Committee.

MTT-5 will be again sponsoring a Student High Efficiency PA Design Competition at IMS 2006. The rules are essentially the same as in 2005.

PA Competition rules are as follows:

1) The PA design may use any type of technology but must be the result of student effort both in the amplifier design and fabrication.
2) The PA mechanical design should allow for internal inspection of all relevant components and circuit elements. The RF ports should be standard coaxial connectors, type N or SMA.
3) The PA must operate at a frequency of greater than 1 but less than 20 GHz, and have an output power level of at least 5 but less than 100 W.
4) All amplifiers should require less than 25 dBm of input power to reach the output level required for maximum efficiency.
5) The PA should require no more than two external dc supply voltages for operation.
6) Amplifier entries should be submitted with measured data, including dc supply requirements, frequency, RF drive and output power, and PAE. PAE will be defined as $(RF_{out} - RF_{in})/dc$. Measurements will be under CW operation at room ambient conditions into a 50-Ω load. Only the power at the fundamental CW frequency will be included in the measurement of output power.
7) The decision will be based solely on the amplifier's PAE measured during official testing at IMS 2006. The judges reserve the right to give favorable consideration for special awards to performance characteristics of special merit, such as higher bandwidth or exceptional workmanship. The decision of the judges will be final.
8) Contestants must notify the MTT-5 committee by e-mailing Dr. Kiki Ikossi (ikossi@ieee.org) of their intention to compete in the contest before 1 April 2006. This notification should include information on the university or educational affiliation of the entry, the faculty advisor, and the PA's approximate power level, dc voltage requirements, and frequency of operation. (Questions about the contest can also be addressed Dr. Ikossi.)

developed using IV and multiple-bias S-parameter measurements, with the aid of Agilent's IC-CAP extraction software. The model was independently validated at high power with a Maury Microwave ATS load/source pull system. The passive surface-mount device (SMD) models for the utilized Coilcraft Air Coil inductors, Toko 0805 Inductors, and ATC 0805 capacitors were supplied by Modelithics. The models were developed from S-parameters measured on multiple substrates in combination with accurate effective series resistance (ESR) measurements [2]. These models have as input parameters the nominal component value and substrate properties (including thickness and dielectric constant), allowing for optimization of component values in Step 8, while fully addressing parasitic effects. These models were added in Step 6, along with microstrip (MS) transmission line models built-in to ADS, after the initial design was completed using Steps 1–5.

Load Pull and Source Pull Simulation

Load pull simulations, enabled by the nonlinear transistor model, were used in ADS to select optimum conditions for high efficiency. The optimal load impedance was determined by initially setting the input impedance to a conjugate gain match. This was done using a 50-Ω simulation using the aforementioned nonlinear model for the Fujitsu FLL120MK [3]. The load- and source-

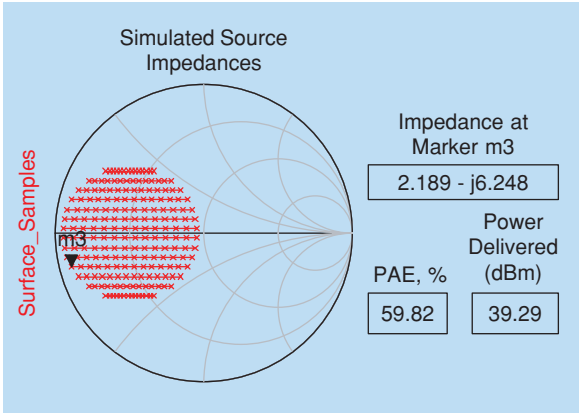


Figure 2. *Source-pull simulation in ADS with the output set to 3.40–j6.48 Ω. Input power is 25 dBm at 1.49 GHz. $V_{ds} = 10$ V, $V_{gs} = -2.0$ V.*

Table 2. Design Process.

Step 0	Establish Suitable Nonlinear Model
Step 1	Determine an Optimum Bias Point, and Load/Source Impedances Using Load/Source Pull Simulation
Step 2	Check S-Parameters and Stability
Step 3	Design Output Matching Network
Step 4	Design Input Matching Network
Step 5	Ideal (Small and Large Signal) Simulation
Step 6	Accurate Passive SMD models with MS T-Line models (Small and Large Signal Simulation)
Step 7	Design Bias Networks
Step 8	Optimize MS T-Line geometries and SMD component values.
Step 9	Layout (and EM simulation)*
Step 10	Measurement
Step 11	Close the Loop (Measured to Simulated Comparisons)

*Post-analysis proved that EM simulation of MS geometries is a potentially important step that should be part of Step 9

The Real World (Nonlinear) Time-Line for the USF Design Entry

Jan.–Mar.

Professor encouragement to first author to enter contest

Student performs some preliminary work and information gathering

Apr.

Entry in the MTT-5 IMS PA design competition (Apr. 6)

Investigated Class E and AB designs

Started Class AB design

May

Worked on the simulation process for a high efficiency design meeting power/gain goals

June(schedule compression!)

(1 June) Panic sets in

(2–3 June) Preliminary design/layout completed

(4–8 June) Simulation iterations/optimizations continue

(9 June) Simulation and layout finalized

(10–11 Jun) Board fabrication

(12 Jun) Assembly

(12 Jun, night) Measurement (grounding problem)

(13 Jun, morning) Redo metal epoxy between heat sink and substrate

(13 Jun, afternoon) Measurement

(13 Jun, night) Prepared presentation

(14 Jun, morning) 2nd Author catches transcontinental flight to Los Angeles with PA successfully shuttled through security

(14 Jun, afternoon) Competition

July

Start 1st paper draft

July/August

Post measurement analysis—"closed the loop"

September

Finalize and submit paper

Advisor (3rd author) comment: As a student project, and the most complete nonlinear simulation/circuit fabrication exercise of its kind yet done at USF, the systematic design procedure proposed in this article was not in place at the outset. Now that it has been benchmarked, we expect a much more efficient design flow for future PA design projects, with the caveat that the importance of attention to details cannot be overemphasized.

pull simulation results are summarized in Tables 3 and 4, respectively. In addition, Figures 1 and 2 show the simulated load- and source-pull results, respectively, for the impedance values providing maximum PAE. A source-pull simulation was then performed, focusing on high-efficiency tuning. Based on iteration of results from load- and source-pull simulation at several different bias conditions, a bias condition $V_{ds} = 10$ V, $V_{gs} = -2.0$ V, and an optimum load impedance were selected. These initial simulations indicated that 59.8% PAE was possible with a source impedance of 2.19–j6.25 Ω and a load impedance of 3.40–j6.48 Ω. A separate harmonic balance (HB) power simulation was performed under the same source/load impedances to confirm the simulation result of PAE = 59.8% and $P_{out} = 39.3$ dBm at an input power of 25 dBm.

Table 3. Load-pull simulation result–freq 1.49 GHz (P_{del} is defined as maximum power delivered from source to load.)

V_{ds} (V)	V_{gs} (V)	Source (Ω)	Load (Ω)	P_{in} (dBm)	PAE (%)	P_{del} (dBm)
	–1.80	1.6–j8.6			57.45	39.28
10	–2.00	1.7–j8.4			59.11	39.09
	–2.20	1.9–j8.0	3.4–j6.5	25	60.71	39.01
	–2.00	1.7–j8.4			61.06	37.53
8	–2.20	2.0–j7.8			62.94	37.47
	–2.30	2.3–j7.2			64.21	37.50

Table 4. Source-pull simulation result–freq 1.49 GHz.

Vds (V)	Vgs (V)	Load (Ω)	Source (Ω)	Pin (dBm)	PAE (%)	Pdel (dBm)
10	–2.00	3.4–j6.5	2.2–j6.2	25	59.82	39.29
		3.5–j7.7	2.2–j6.2	27	59.65	40.61
				28	59.22	40.71
10	–2.20	3.4–j6.5	2.2–j6.2	25	59.09	39.06

Design and Simulation of a Matched Amplifier

The ADS DesignGuide tool, "Lumped Multi-Element Z-Y Matching Networks," was used to determine lumped element output and input matching networks (MNs) [4] that transformed 50 Ω into the desired optimum load and source impedance values. Figures 3–5 show the ideal MNs and results.

Both small- and large-signal simulations were next performed with ideal passive components used to realize the required matching. A 10-V drain-source voltage and a −2.0-V gate-source voltage were used for the initial transistor bias. Figure 6 shows the small-signal simulations. The result shows 16.2-dB gain at 1.49 GHz, which satisfies the design goal in Table 1.

Large-signal simulation was performed using a template under the "DesignGuide" from the ADS schematic window. Figure 7 shows the ideal large-signal simulation schematic. The result in Figure 8 shows 62.2% PAE, output power of 39.38 dBm, and input power of 25 dBm. These results are slightly better than those achieved under the initial load/source pull simulation.

The substrate-scalable and part-value-scalable SMD models were next combined with transmission-line models using built-in ADS elements, MS line (MLIN), MS step (MSTEP), and MS TEE (MTEE). The 50-Ω width for MS line was calculated by the ADS transmission line calculator, LineCalc, to be 2.86 mm. These calculations were based on 59 mil thick FR4 substrate information (Er = 4.3).

Optimization Using Scalable Parasitic Models

Optimization of component values and MS line geometries is necessary to achieve the required performance in a fabricated amplifier. Optimizations and goals were selected under the component pallet list of ADS. The input and output MN were separately optimized based on the optimum load and source

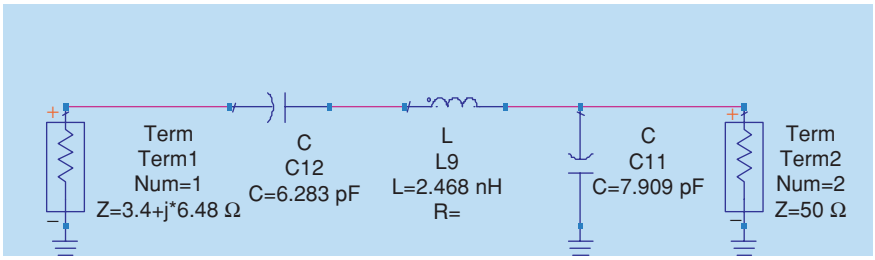


Figure 3. *Schematic of ideal MN for matching the load impedance (3.40 + j6.48) Ω to 50 Ω.*

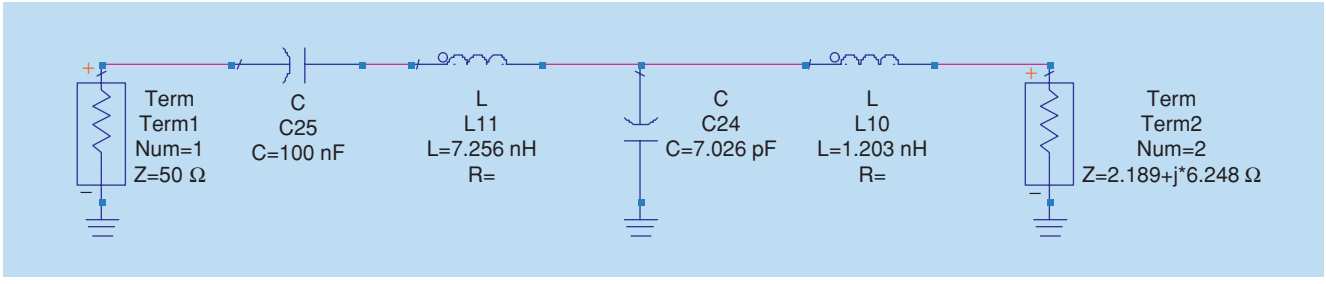


Figure 4. *Schematic of ideal MN for matching the source impedance, (2.2 + j6.2) Ω, to 50 Ω.*

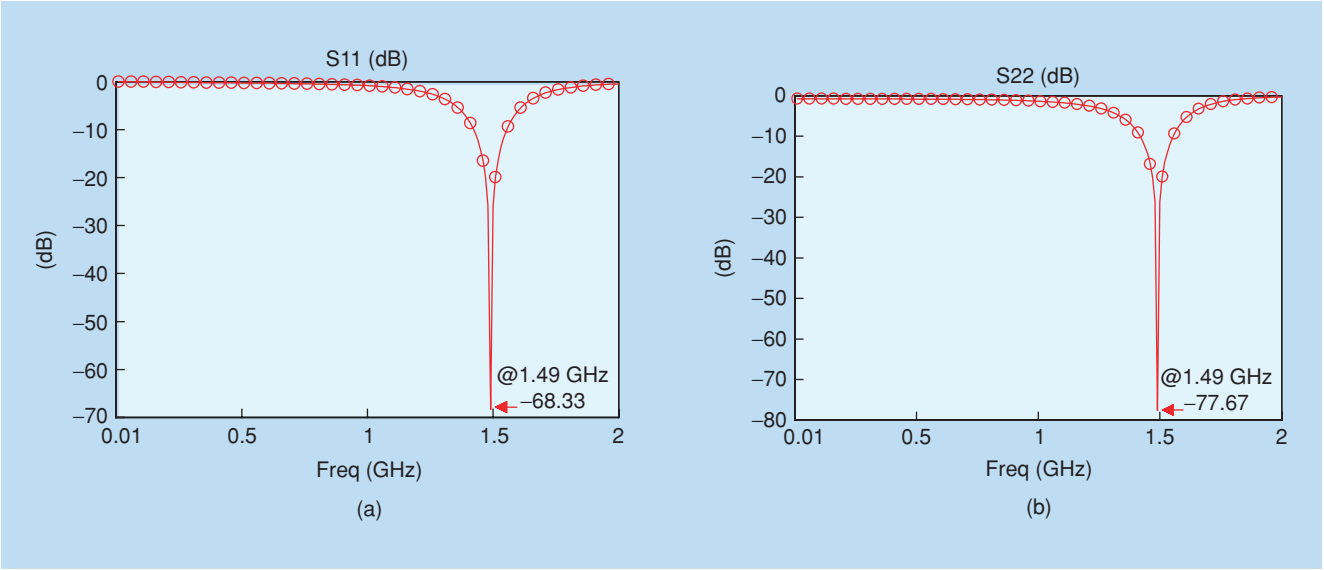


Figure 5. *(a) Simulation of the ideal output matching network and (b) input matching network, based on the schematics shown schematically in Figures 3 and 4, respectively. These results validate the transformation to the desired input/output matching conditions.*

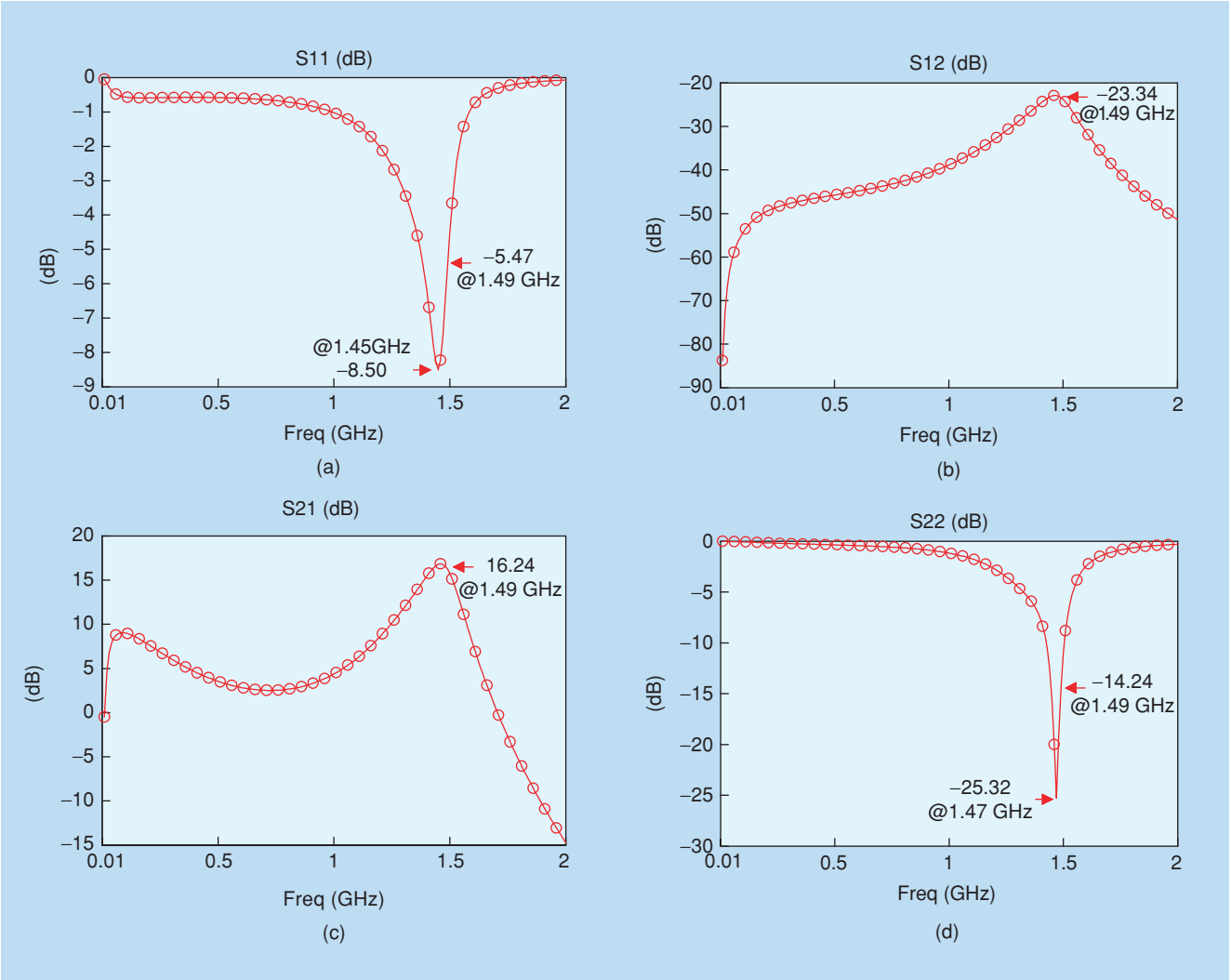


Figure 6. *Class AB amplifier results using ideal lumped elements for matching. Results show good gain and impedance matching at the originally targeted 1.49 GHz.*

impedances (see Figures 1 and 2). The width and length of the MS transmission lines and SMD component values were both optimized to achieve the required impedances. This was done in three steps. First, both transmission-line dimensions and component values were allowed to vary across a continuous range. Second, the closest available SMD component values (chosen from the vendor's available parts list) were entered into the simulation. Third, a final optimization was executed, allowing only the transmission-line dimensions to provide a best fit to desired match conditions. An alternative approach would be to set up a discrete optimization with respect to the available SMD component values, in which case the optimization could be performed in one step.

Figures 9–12 show the optimized schematics for the output and input MNs. Both small- and large-signal simulations were performed after optimization. Simulated results indicated 56% PAE at 38.6 dBm output power was achievable at 25 dBm input power. This corresponds to 14.9-dB small-signal gain for these simulations that were performed at $V_{ds} = 10$ V, $V_{gs} = -2.0$ V condition. (Later, we'll see that some adjustment of bias condition will lead to even better efficiency on the bench.) Layouts were then generated automatically from the schematic using ADS, producing the layouts of Figures 11 and 12. These layouts were used directly to fabricate the circuit using an LPKF [8] milling machine at USF. Figures 13 and 14 show the nonlinear simulations of the optimized design.

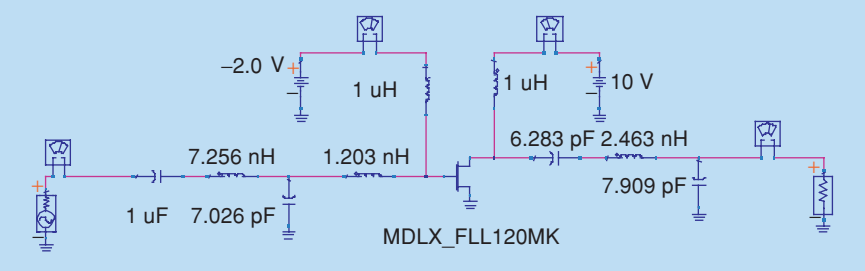


Figure 7. *Ideal large signal simulation schematic used for harmonic balance simulations in ADS. This network combines the ideal lumped matching networks from Figures 3 and 4 with the nonlinear transistor model and ideal bias T network and was used to generate the large-signal simulation results of Figure 8.*

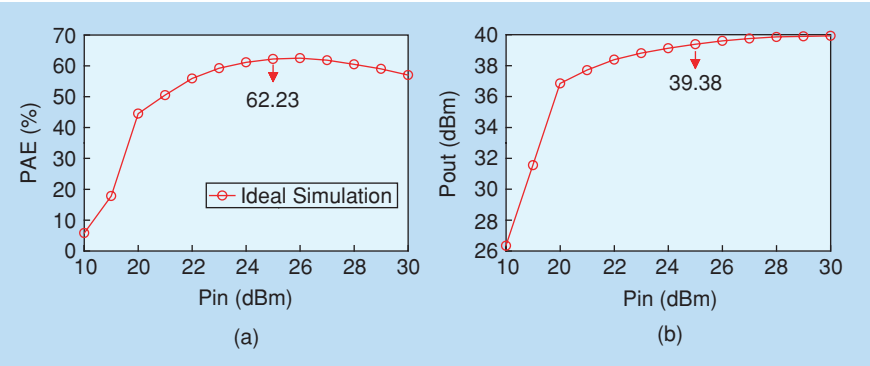


Figure 8. *Large signal simulation results for transistor with ideal matching networks at a bias condition of 10 V, V_{ds}, and −2 V, V_{gs}.*

Measurement Results

The completed assembled class AB PA was shown in Figure 15. Metal epoxy was used to create the via grounding and connection between the circuit board and heat sink. The small- and

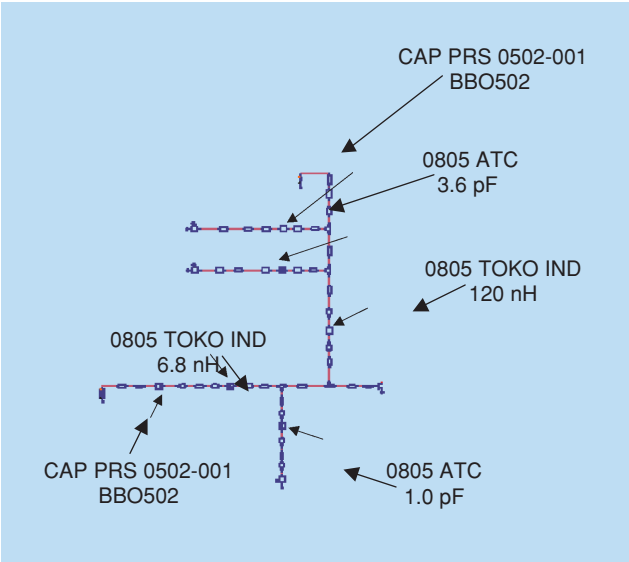


Figure 9. *Input schematic containing transmission line elements and component models tuned to values to provide optimal circuit performance.*

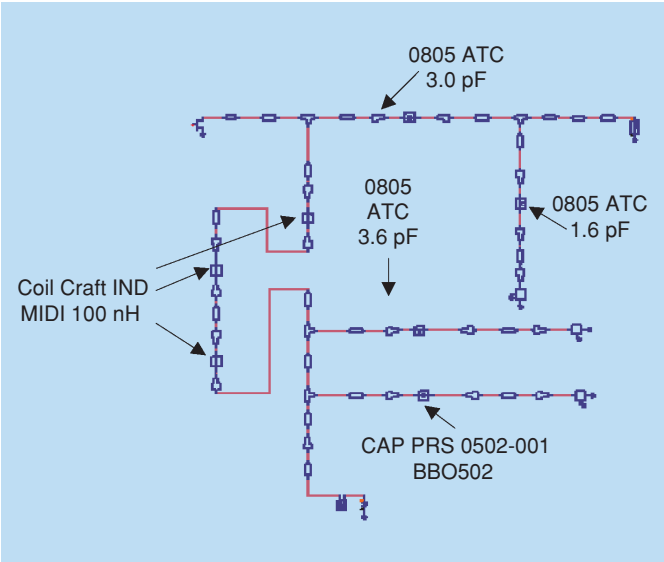


Figure 10. *Optimized output schematic containing transmission line elements and component models tuned to values to provide optimal circuit performance.*

large-signal measurement results showed the peak gain frequency was shifted down around 200 MHz. Further analysis later in this article fully explains this shift, but all other goals, including PAE, the required power level, and gain were achieved without bench tuning.

S-parameters were measured using an Anritsu 37397C Vector Network Analyzer calibrated with a K-connector SOLT calibration kit. The S-parameter results showed 13.6-dB gain at 1.29 GHz. As explained in the following section, the frequency shift (to 1.29 GHz) observed for the measured amplifier, as compared to the initial design center frequency, was found to be due to a misinterpretation of the reference plane location on the transistor model. Correcting for this effect produced excellent simulation to modeled agreement for all parameters.

Figure 16 shows the measurement test configuration used at USF for power measurements. A Maury microwave automatic tuner system (ATS) was used to facilitate the power sweep measurement. In this nonlinear test, 54.5% efficiency was achieved at 25-dBm input power (10-V V_{ds}, –2.2-V V_{gs}), however, the voltage drop due to the drain bias cable was not taken into account in this initial measurement. By using an adjusted bias condition, V_{ds}, an efficiency of 61.7% was measured at the 2005 IEEE MTT-S Symposium in conjunction with the PA design competition.

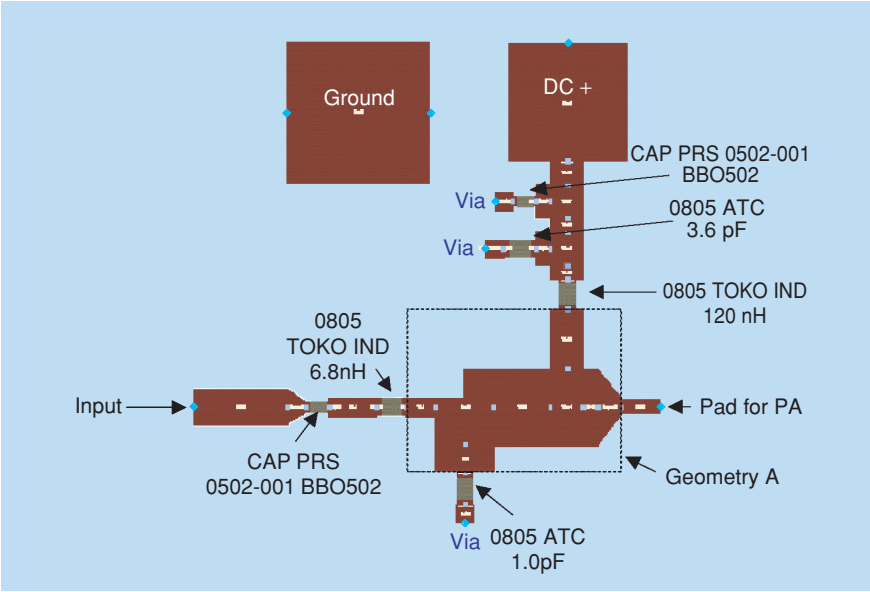


Figure 11. *Layout (generated automatically in ADS) of the input MN whose schematic is shown in Figure 9.*

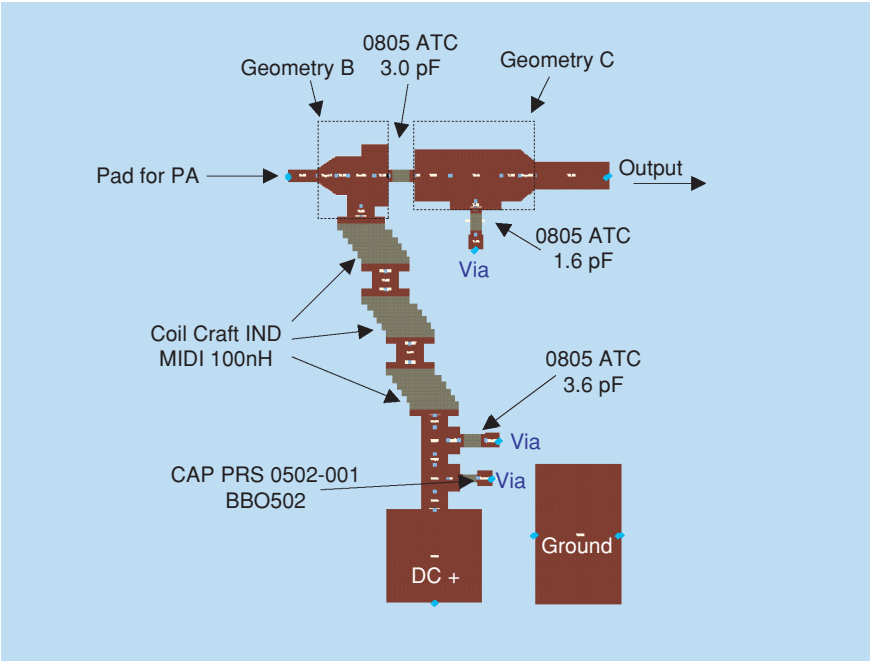


Figure 12. *Layout (generated automatically in ADS) of the output MN whose schematic is shown in Figure 9.*

Closing the Loop —Post-Measurement Analysis

A careful analysis was performed to understand the 200-MHz frequency shift observed in the measured versus simulated amplifier. Exploration included careful examining of via-hole models and more accurate representation of MS matching elements using electromagnetic (EM) analysis, however, a careful review of the interface between the MS circuit and the transistor revealed that the main problem was a misinterpretation of the reference plane location on the transistor model. The modeled transistor measurements were made with the device embedded between small sections of 50-Ω line on a 10-mil GTEK FR4[d1] substrate (Er = 3.8). The amplifier was fabricated on a 59-mil FR4 substrate (Er = 4.3).

The result using the corrected schematic, with the 10-mil GTEK line sections properly de-embedded, shows the resonant frequency shifted down to 1.33 GHz. Further improvement in measured to simulated agreement was achieved with the aid of EM analysis using a Sonnet EM simulator [9]. The EM analysis S-parameter results of geometry A, B, and C, shown in Figures 12 and 13, were implemented into the ADS simulation schematic. Combining the EM simulation for these MS portions of the input- and output-matching sections centered the simulated gain at 1.29 GHz. Figure 17 shows the comparison result including the EM simulation.

Final Comparisons

Figures 18–20 show the comparison result between the measurement and simulation using the original design bias condition (10-V V_{ds}, –2.0-V V_{gs}).

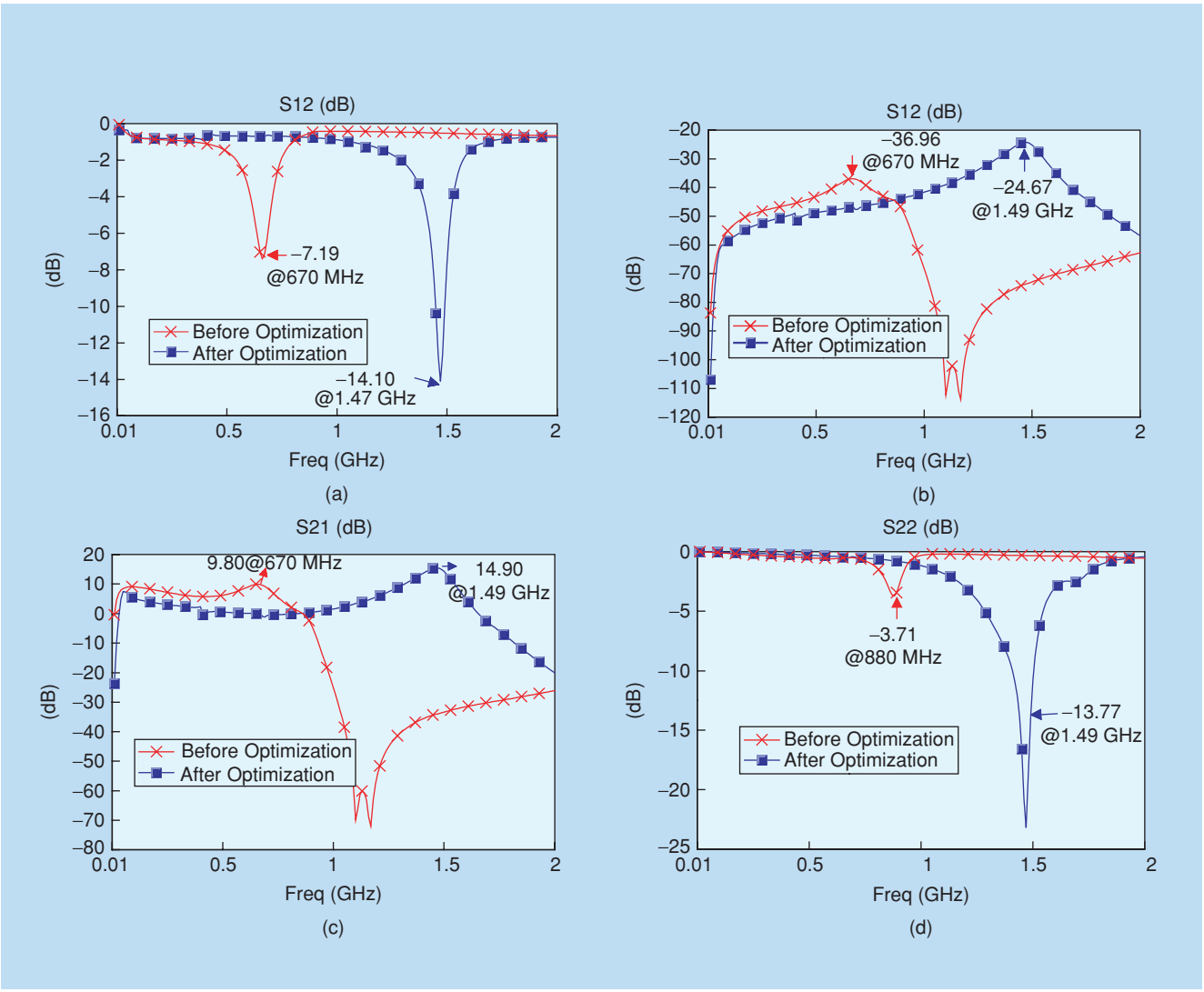


Figure 13. *Small signal simulation results using passive SMD models along with ADS MS models before and after optimization.*

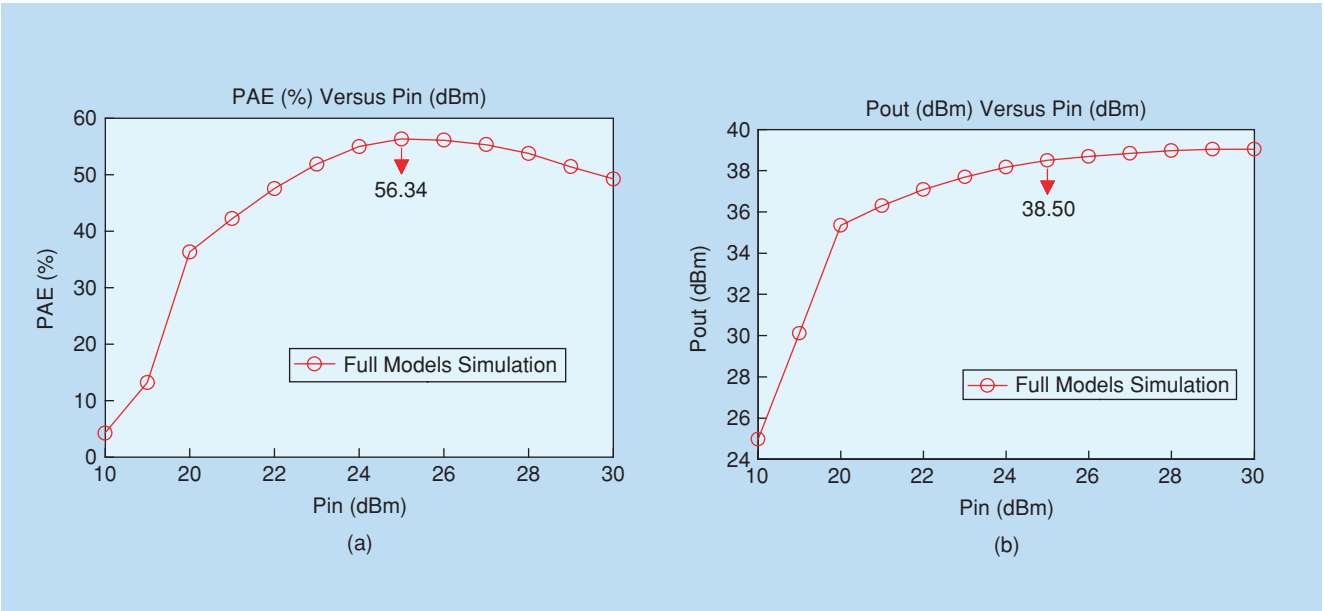


Figure 14. *Large signal simulation results for optimized circuit at 1.49 GHz for the bias condition of 10 V, Vds, and −2 V, V_{gs}.*

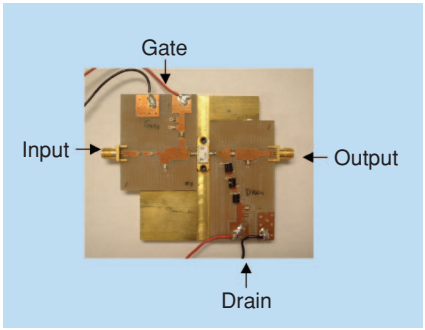


Figure 15. *PA assembled from the fabricated input and output circuits whose layouts were shown in Figures 11 and 12, respectively.*

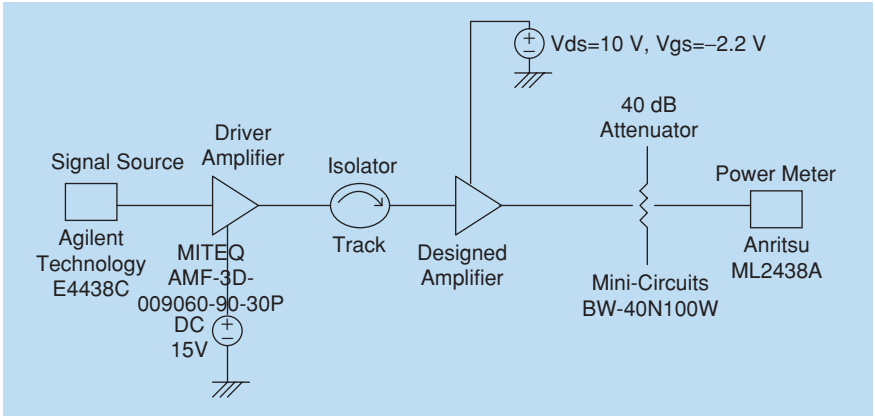


Figure 16. *The USF PA measurement test configuration.*

The small-signal comparison in Figure 18 shows good agreement is seen for all four S-parameter magnitudes. The gain is slightly lower, which could in part be due to the fact that connector loss was not de-embedded from the measurements, and there could be some radiation loss due to the MS elements. Figure 20 shows excellent measured-to-simulated agreement for the power and efficiency. Figures 21 and 22 show 59% PAE is achieved for both simulation and measurement, with a bias condition closer to that used at the competition. Excellent agreement was again

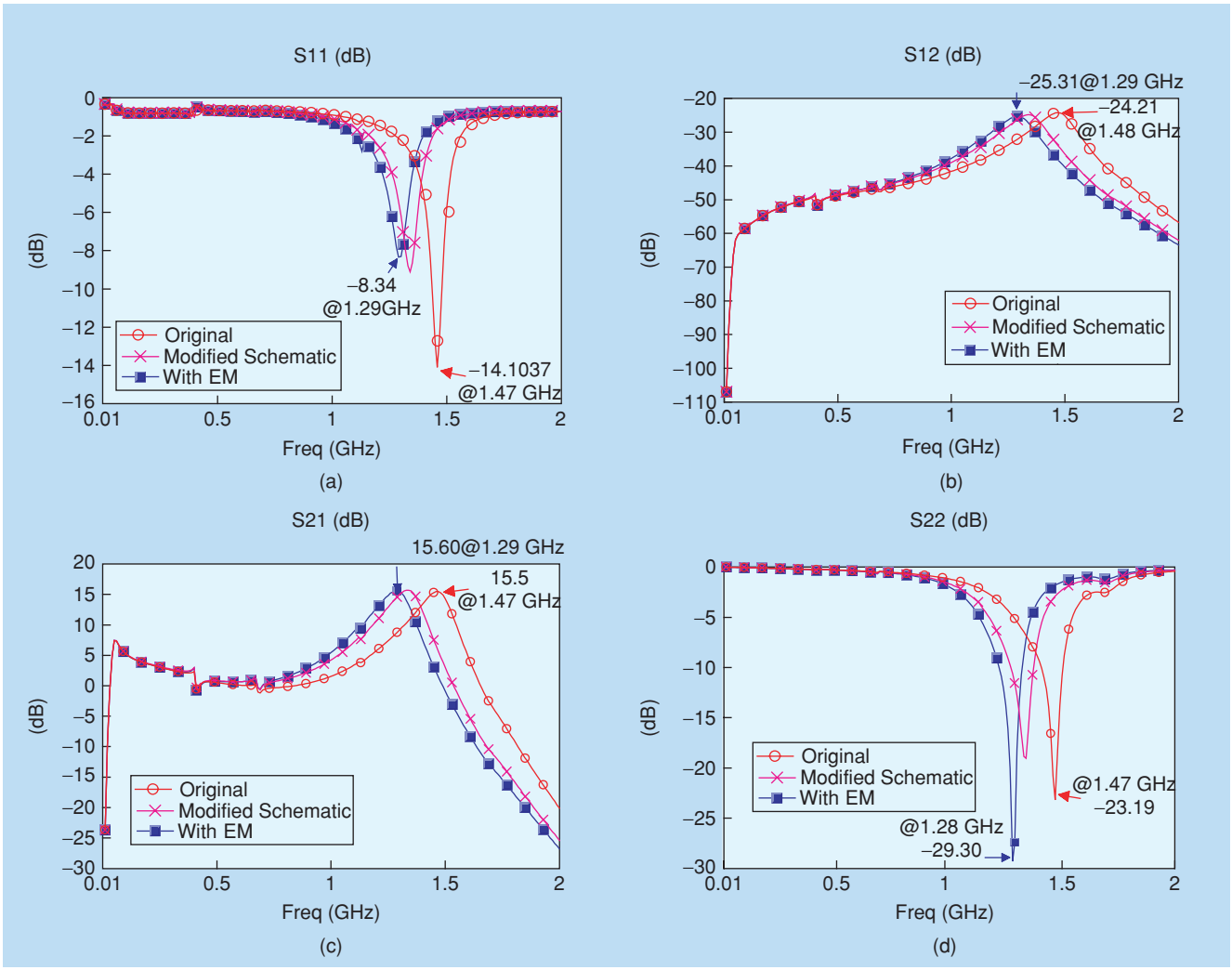


Figure 17. *S-parameter result comparison including the EM simulation of the amplifier shown in Figure 15. (Bias condition is 10 V, V_{ds}, and −2.0 V, V_{gs}).*

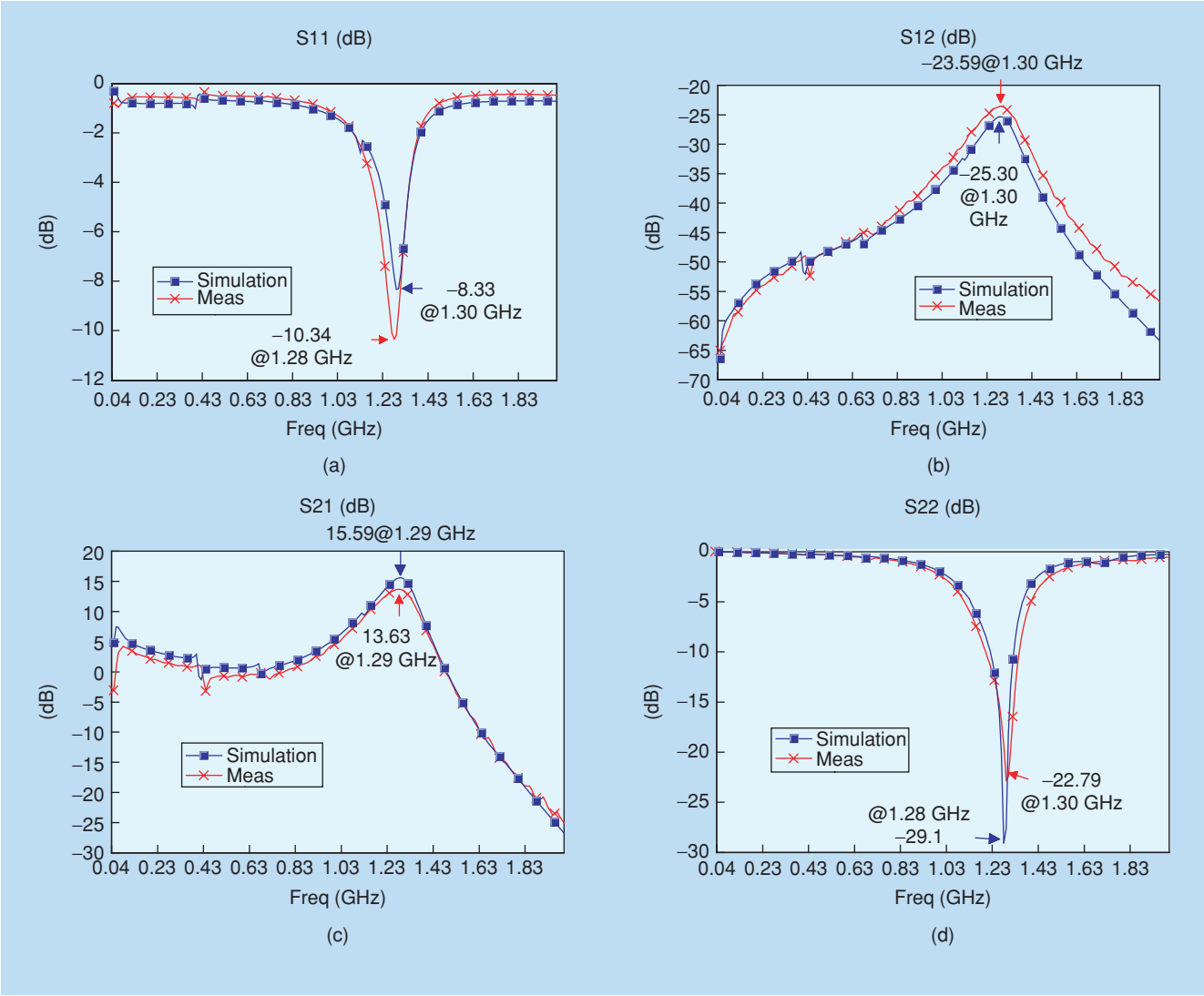


Figure 18. *S-parameter result comparison for amplifier in Figure 15 at bias of 10 V V_{ds}, −2.0 V V_{gs} (700 mA I_{ds}).*

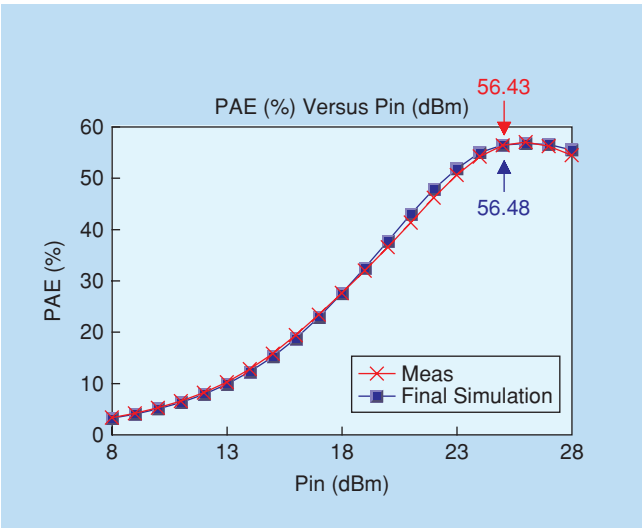


Figure 19. *Measured PAE result for amplifier in Figure 15 at bias points of −10 V V_{ds}, −2.0 V V_{gs}.*

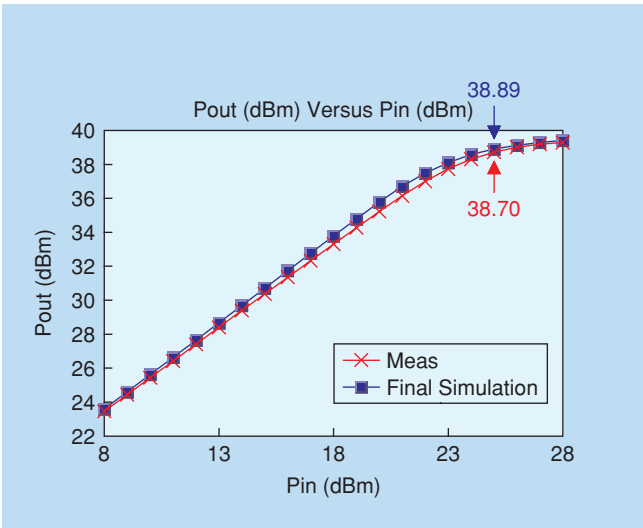


Figure 20. *Pout versus pin measurement result for amplifier in Figure 15 at biases of −10 V V_{ds}, −2.0 V V_{gs}.*

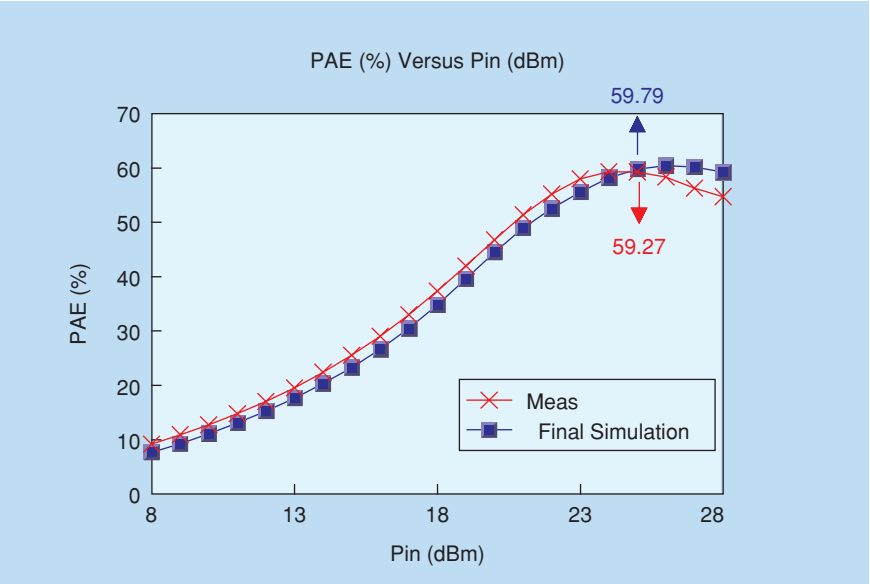


Figure 21. *Measured PAE for amplifier at −8 V V_{ds}, −2.2 V V_{gs}.*

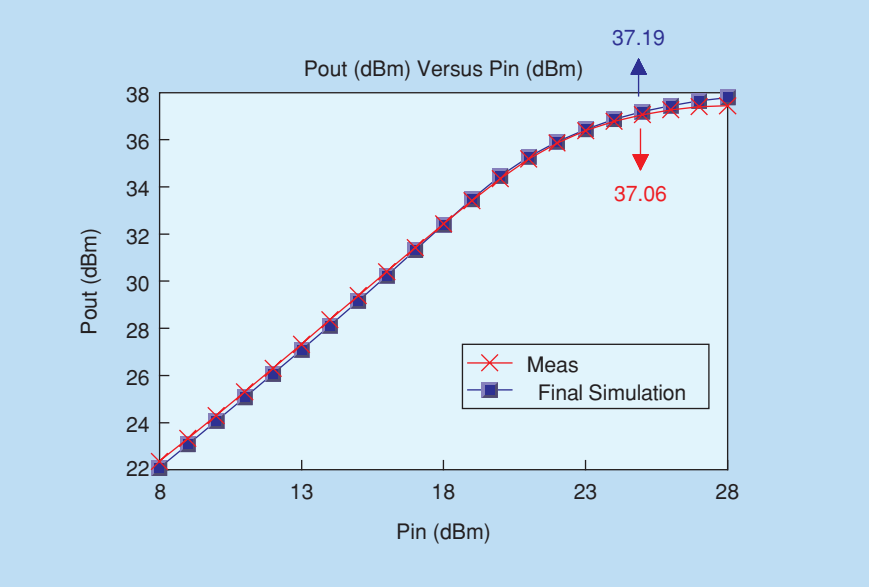


Figure 22. *Figure 22 measured pout versus pin for amplifier at −8 V V_{ds}, −2.2 V V_{gs}.*

observed between measured and simulated large-signal results. The difference between the 62% observed at the competition and this result is attributed to differences in the test setup and possible differences in the exact bias condition achieved at the device terminals.

Summary

A Class-AB PA application circuit targeting 1.5 GHz was introduced and benchmarked a systematic design procedure enabled by use of high-accuracy models for active and passive circuit elements. A Fujitsu FLL120MK GaAs FET device was chosen to satisfy the power, efficiency, and gain design goals. Load- and source-pull simulations were performed using a customized nonlinear model for the transistor within ADS to find an optimum bias condition, along with a load and source impedance that enabled high efficiency at the required 25-dBm power input level. The nonlinear transistor model and passive-surface mount device models from Modelithics were used, along with built-in MS line models in ADS to accomplish the design optimization and simulation. PAE of 60% and output power of 37.06 dBm with input power of 25 dBm were obtained at 1.29 GHz. This measurement result showed that the frequency shifted around 200 MHz. A misinterpretation of the transistor model reference plane location caused the frequency shift. After including the corrected schematic and adding EM simulation for the MS matching sections, excellent agreement was obtained between the simulation and measurement at the two different bias conditions analyzed. This work sets the stage for a more efficient simulation-based design flow for PA design that relies on accurate models. It also underlies the importance of attention to detail in setting up simulations and proper use of the various simulation, measurement, and model extraction tools available.

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