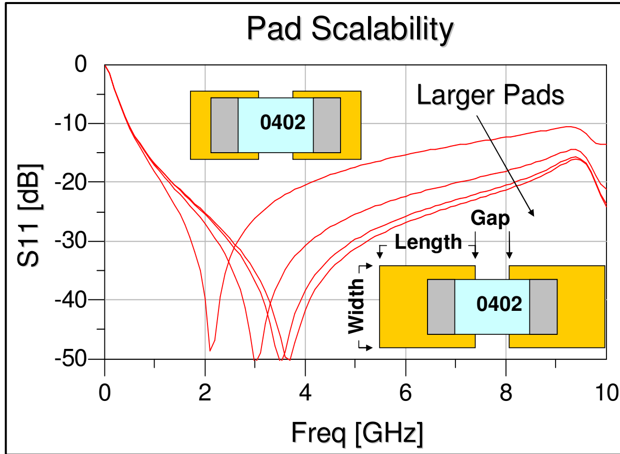


Pad Geometry Scaling and Removal in Advanced Capacitor Models

Solder pad geometry can have a strong influence on the parasitic behavior of surface mount components. Careful treatment and accounting for actual pad geometries can lead to excellent simulation results.

Pad scalability corresponds to the ability to change the dimensions of the bonding or solder pad used for attachment of a surface mount component. In this paper, a new pad scalability feature added to selected Global Models contained in Modelithics CLR Library[1,2] is discussed. We demonstrate the excellent correlation between high frequency measured data and simulated performance by using ATC capacitors and corresponding models. Some interesting features such as arbitrary pad shape simulation and new statistical analysis are also explored. The pad scalability feature will become available in an increasing number of Modelithics models in future releases of the library.

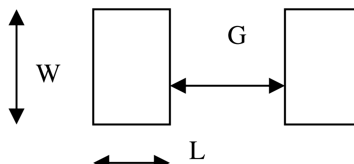
There are two methods available in the Modelithics CLR Library for addressing the pad stack effects. The first method is associated with what are termed “pad scalable” models, which currently comprise a sub-set of the overall CLR Library that includes models for the ATC 600L, 600S, 600F and 545L series. In these models, user-level input parameters are provided that define the pad size and spacing. Limits are provided in the model descriptions to indicate the range of validity for the pad dimensions (typically based on IPC standards). The second method, which applies to all models in the CLR Library, is available by setting the Sim_mode input parameter to 2; this setting causes all pad-related effects to be ignored (while retaining all other parasitic effects) and effectively puts the reference plane at the outer edges of the component. When using the Sim_mode = 2 approach the user is responsible for substituting appropriate pad-related effects. Of the two methods, the “pad scalable” approach is generally more accurate since precise segmentation of component and pad-related parasitics is more difficult to achieve but a necessary assumption when using the Sim_mode = 2 method.

To illustrate the pad scalability feature, two sets of pad dimensions were used for two ATC capacitor families, 600S and 600L. The dimensions of the pads are given in Table 1. Along with comparisons between the measured and simulated performance for different pad sizes, the pad removal (Sim_mode=2) feature is reviewed to illustrate how arbitrary pad shapes can be simulated.

Table 1 - Pad dimensions used in this study (mils). Refer to Figure 1 for definitions of parameters.

Part	PAD A			PAD B		
	Width (W)	Length (L)	Gap (G)	Width (W)	Length (L)	Gap (G)
ATC 0402 (600L)	20	13	14	33	18	16
ATC 0603 (600S)	33	20	20	45	30	24

Figure 1 - Pad dimension definition



S11 [dB]

Pad Variation Results for ATC 0603 600S Capacitors

In Figure 2 and Figure 3, measurement and model simulation results are given for ATC 600S capacitors mounted in series on 15 mil-thick TMM10i (er ~ 9.8) using the small (Pad A) and large (Pad B) pad stacks. As would be expected the larger pads lead to a reduction in the return loss and increased insertion loss, due primarily to higher capacitive-coupling to ground. The effect is more pronounced for the smaller capacitor (Figure 2) since the loading effect of the shunt reactance is greater with higher series reactance.

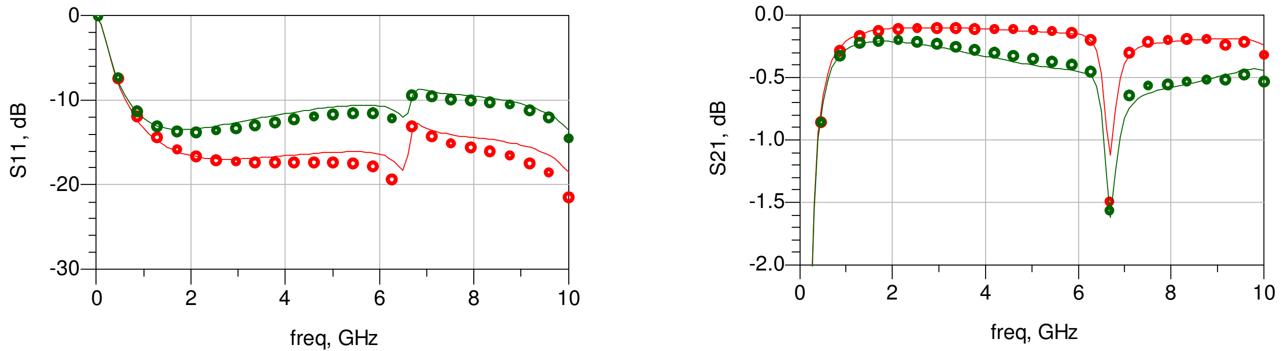


Figure 2 – 8.2 pF ATC 0603 capacitors on 15 mil TMM10i board. Legend: Pad A – Red line, Pad B – Green line. Model - solid lines; Measured data - markers.

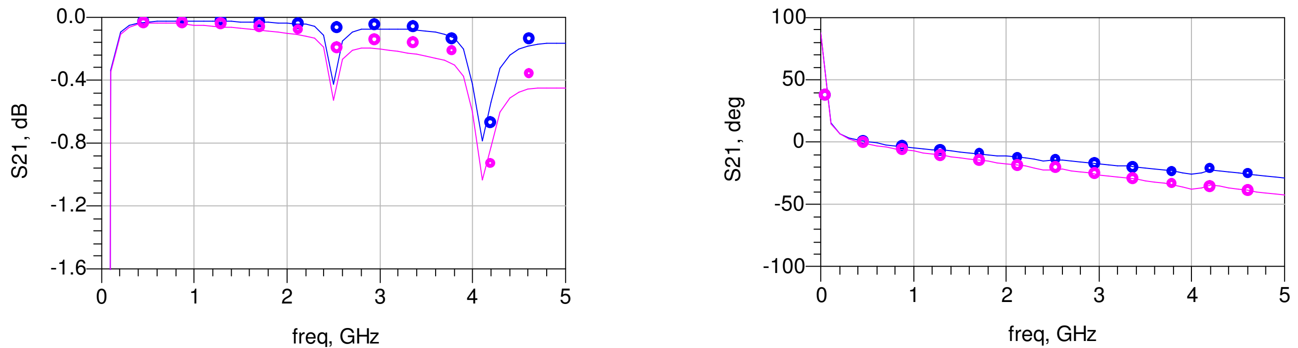


Figure 3 – 56 pF ATC 0603 capacitors on 15 mil TMM10i board. Legend: Pad A – Blue line, Pad B – Pink line. Model - solid lines; Measured data - markers.

Pad Variation Results for ATC 0402 600L Capacitors

Figure 4 and Figure 5 show measurement-to-model comparisons for ATC 600L capacitors mounted in series using the two pad dimensions given in Table 1. In this case a 4 mil-thick Rogers 4350 (er~3.5) substrate was used. The main difference in the pad dimensions is in the pad width (see Table 1), and while the insertion loss varies by only 0.1-0.2 dB below the parallel resonance, there is a large variation in the return loss. The results

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shown here, and previously in Figure 2 and Figure 3, indicate that larger variations based on pad dimensions will occur for smaller part values.

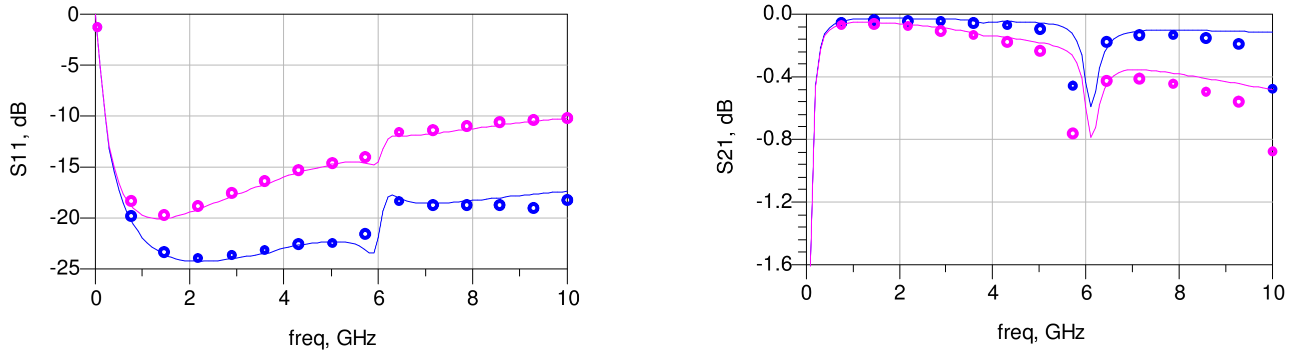

Figure 4 – 8.2 pF ATC 0402 capacitors on RO4350B 4mils board. Legend: Pad A – Blue line, Pad B – Pink line. Model - solid lines; Measured data - markers.

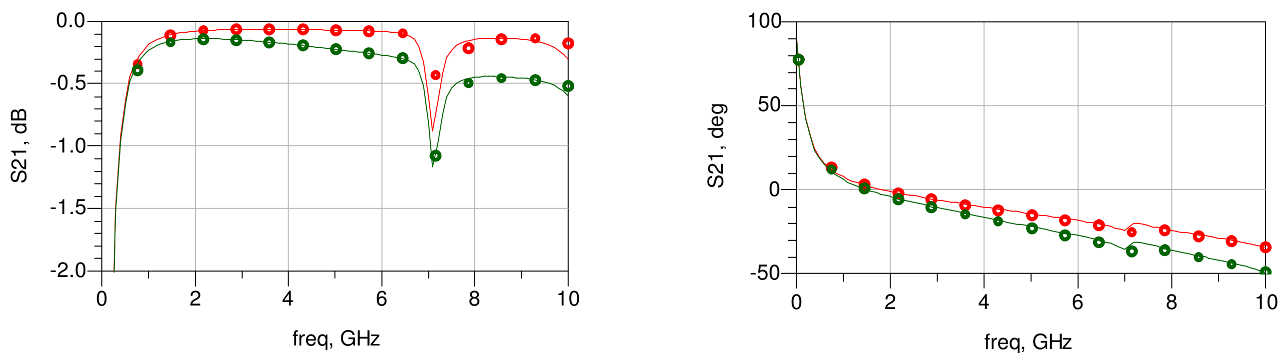

Figure 5 – 24 pF ATC 0402 capacitors on RO4350B 4mils board. Legend: Pad A – Red line, Pad B – Green line. Model - solid lines; Measured data - markers.

Pad Removal

Another useful feature in the CLR Library, that is available for all models, is the ability to use arbitrary pad shapes and dimensions for bonding pads. This can be done by setting the model to Sim_mode=2 and attaching the required pad externally. A representative schematic is illustrated in Figure 6. When Sim_mode=2 the reference planes are shifted to the outer edge of the component, as opposed to being located at the outer edges of the mounting pads in the default (e.g. Sim_mode=1) setting . As the bonding pad is completely de-embedded, arbitrary pad size and shapes can now be simulated.

Figure 7 shows the layout of the pads that were used in the ADS-Momentum simulation. The bonding pad was split into two separate sections and simulated as separate designs. Section 1 corresponds to the portion of the pad that is not overlapped by the component while section 2 indicates the overlapped portion. The numerical EM simulation was called into the ADS circuit simulator as a co-simulation; as seen in Figure 8 there is excellent agreement between the original model with built-in pad effects (Sim_mode=0) and the results when the pads are substituted with the EM simulation data (Sim_Mode=2). The usefulness of this method, of course, is the ability to utilize custom pad dimensions with the Modelithics models.

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An alternative approach to EM co-simulation that is possible with many electromagnetic simulation tools is to use what is often referred to as an “internal port” and simulate the pad as one piece rather than two. Using this approach a standard port would be used at the outer edge of a pad and the internal port would be placed on top of the pad, at the assumed mounting location for the SMD (corresponding to the outer edge of the SMD). The implementation of internal ports is done differently depending on the EM simulation tool, and for this demonstration the more generic method of splitting the pad into two pieces was used. Note that pad-to-pad coupling, while not a predominant parasitic effect, is still accounted for in the models when using Sim_mode=2.

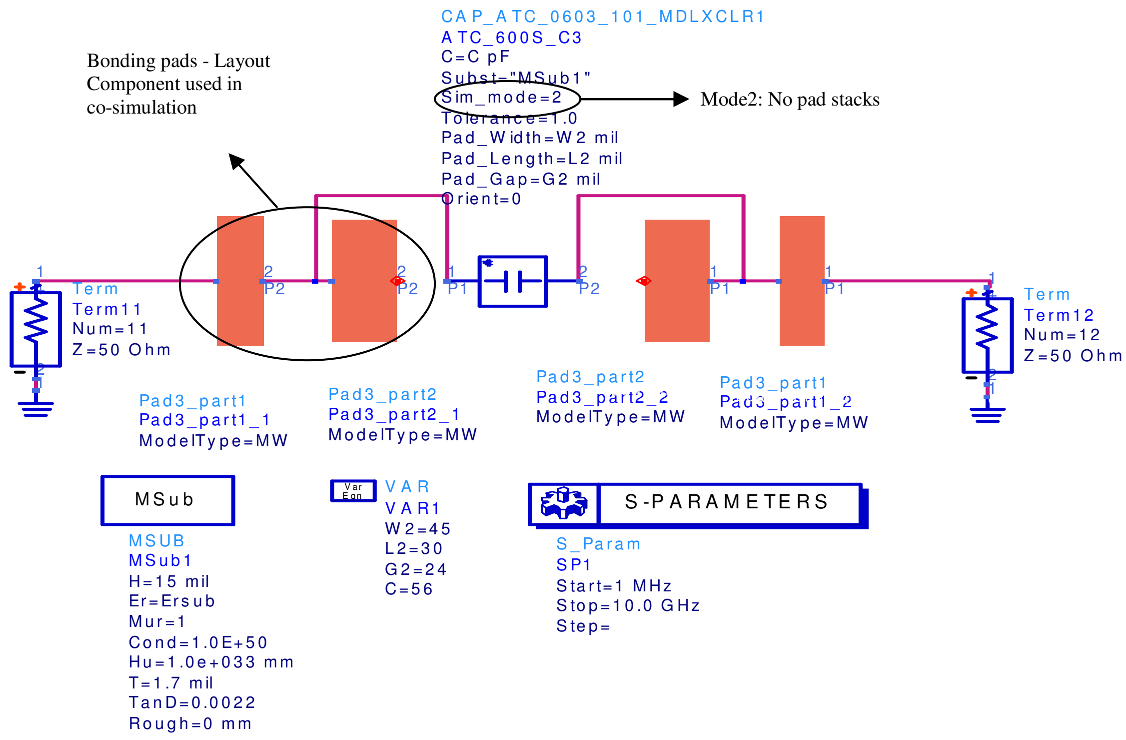

Figure 6 – Schematic used to demonstrate Sim_mode = 2 (no pad stack option) in the Modelithics CLR Library

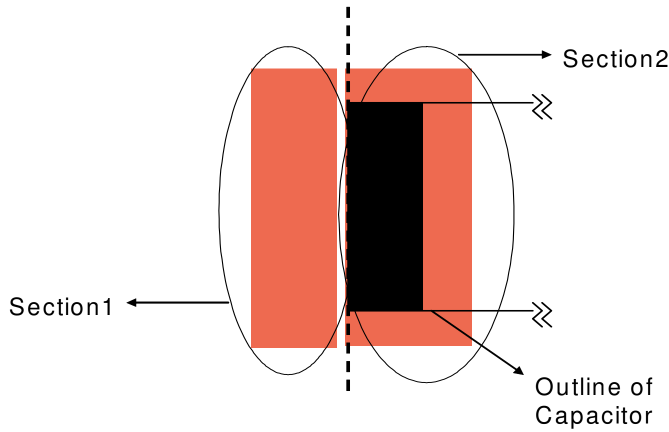

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Figure 7 - Outline of the layout that was used in *Momentum* (MoM) to simulate the bonding pads.

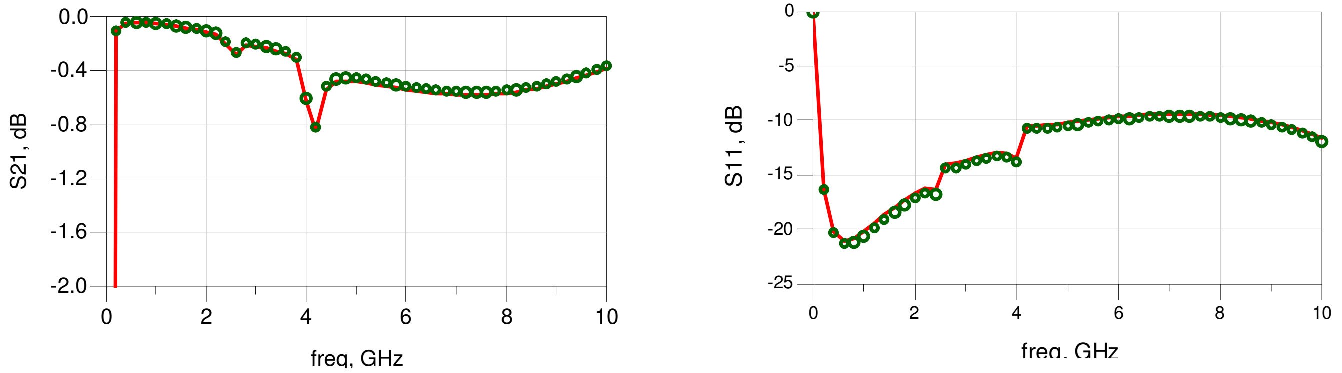

Figure 8 – Comparison between Sim_Mode = 0 (built-in pads from the model) and Sim_Mode = 2 with pads simulated using *Momentum* (MoM). Legend: Mode 0 – Solid line, Mode 2 – Markers.

Pad-width, Substrate Height Sensitivity and Monte Carlo Analysis

Figure 9 illustrates the sensitivity of S21 to the pad width. The lines with the markers correspond to measured data for 8.2pF ATC 0402 capacitors on an RO4350B 4 mil-thick board. The yellow line corresponds to simulated data for different pad-width dimensions. The width of the pad was varied from 18 to 40 mils while the length and gap was kept a constant at 13 and 14 mils, respectively. It is interesting to note that the pad length and the pad gap had minimal effects on the simulation.

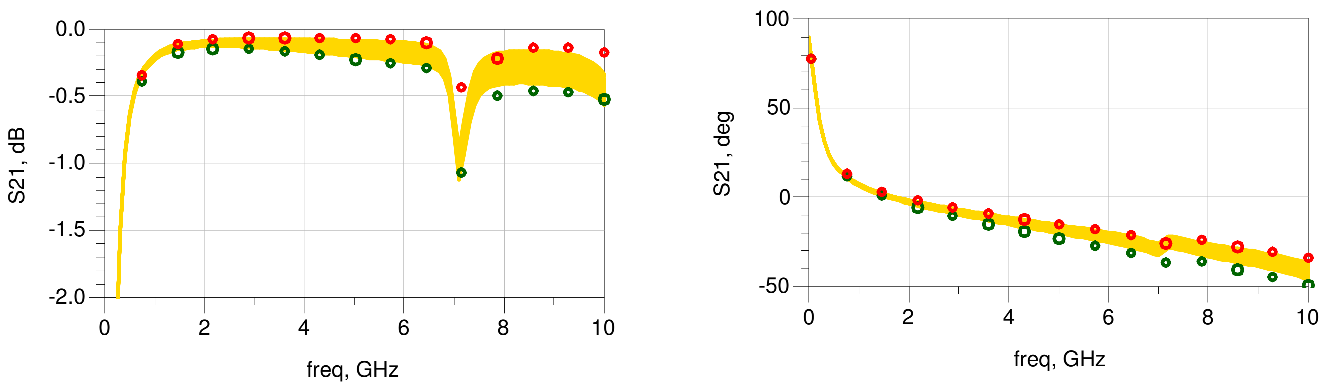

Figure 9 – Pad-width sensitivity analysis. Comparison between measured data (scatter plot) and simulation (yellow) for different pad widths. Red marker – Pad A, Green marker – Pad B.

Another interesting observation is as the substrate becomes thicker the PCB parasitic effects become smaller, so the pad dimensions play a less dominant role. Also, as discussed before, as the capacitance value becomes larger the effects of the pad dimensions decrease. Figure 10 and Figure 11 show the difference in the insertion loss at 4GHz, for two different pad-sizes (Pad A and B), against substrate height and capacitance value, respectively. The simulation was performed for 8.2pF ATC 0603 caps mounted on TMM10i board. Please refer to Table 1 for pad dimensions.

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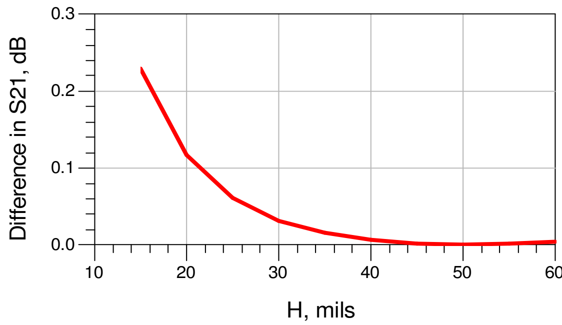


Figure 10 – Substrate height sensitivity analysis at 4 GHz – difference between Pad A and B versus substrate height using an 8.2 pF capacitor on TMM10i.

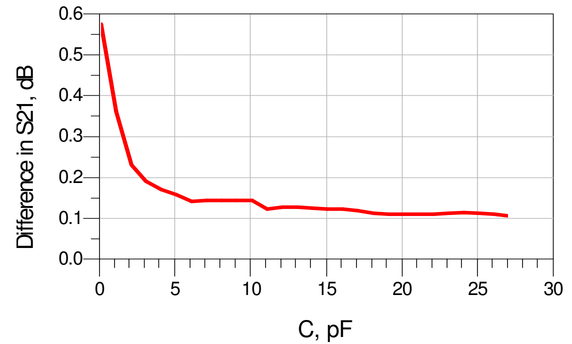
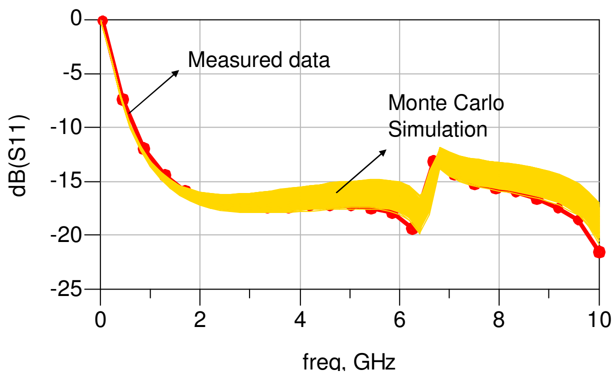


Figure 11 – Capacitance sensitivity analysis at 4 GHz – difference between Pad A and B versus capacitance value using 15 mil-thick TMM10i.

In addition to part value tolerances, with the new pad-scalable CLR models statistical analysis which includes the substrate and the pad dimension variations can also be performed. Figure 12 shows the result of one such Monte-Carlo simulation for 8.2pF ATC 0603 caps mounted on TMM10i board. The simulation settings that were used: Width =30-36 mils, Length = 18.5-21.5 mils G= 17-23 mils and er=9.8+/-0.23.



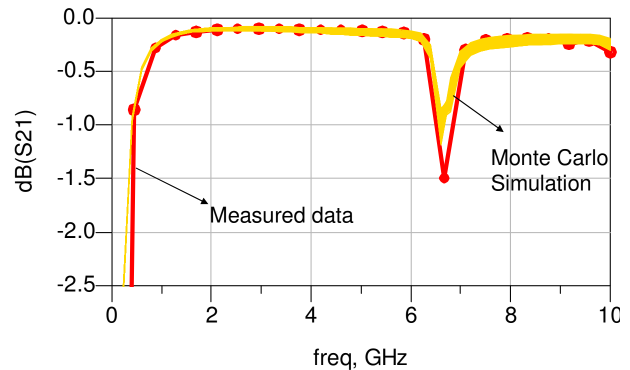


Figure 12 – Monte Carlo Analysis.

Summary

Enhanced capacitor models are described that flexibly address the effects of solder pad geometries on surface mount capacitors.

Pad scalable models allow the designer to conveniently specify the geometries of pads to be used in application that may be differ from those used to characterize and model the component. pad removable model features allow maximum flexibility in allowing users, for example, to combine use of EM analysis of alternative pad geometries to be combined with the use of advanced Modelithics capacitor models.

http://www.modelithics.com/free-models.asp

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REFERENCES

[1] "Advanced Microwave Chip Capacitor Models *Microwave Journal*, January 2002.
[2] "Comprehensive Models for RLC Components to Accelerate PCB Designs," *Microwave Journal,* May 2004.

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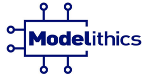

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