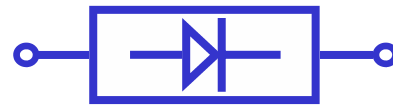


surface mount PIN diode model



Model Features

- Frequency range: (DC-4 GHz)
- Substrate scalable
- Non-linear equivalent circuit topology
- Measurement validations:
 - DC-IV
 - Capacitance vs voltage
 - Resistance vs DC Current
 - Single tone Harmonics
 - Multi-bias S-parameters
 - Time domain



Microsemi UPP9401 PIN Powermite Package

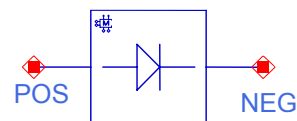
Model Description

The PIN-MIC-PMITE-001 is a substrate scalable and bias dependent non-linear model for the Microsemi UPP9401 single PIN diode in a powermite package. The model is intended for use with microstrip applications operating from DC to 4 GHz. Users specify substrate height, dielectric constant, loss tangent, and interconnect metal thickness. Both junction capacitance and RF resistance are modeled as a function of bias. The part is designed for use in two-way radio antenna switch applications.

Technical Notes

- Two-port series S-parameter measurements were made using a vector network analyzer and on-board probing with calibration referenced at the component pad-stacks.
- The model has been validated over a bias range of -20 to 0.9V.
- The reverse and forward-bias C-V data was measured using a LCR meter.
- The reverse and forward-bias IV data was measured using a Keithley 4200 SCS system.
- Resistance as function of DC current was measured using a LCR meter.
- Substrates used to extract the models: 4 mil Rogers 4350, 14 and 59 mil-thick FR4.
- Typical range of valid substrate types (substrate height H in mils and dielectric constant Er): $1 \leq H/Er \leq 16$.
- Further Microsemi PIN diode information is available at www.microsemi.com

Model Representation

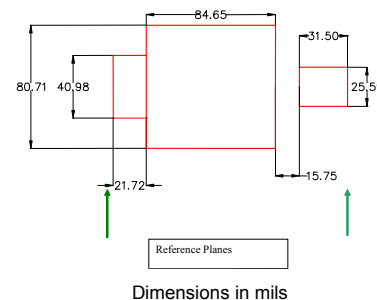


PIN_MIC_PMITE_001

MDLX_DIO1

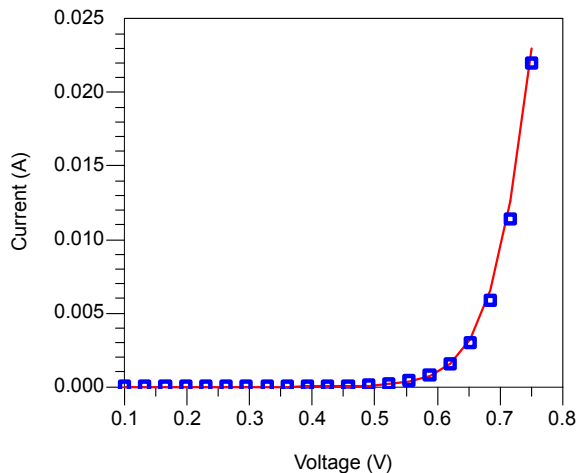
Subst="MSub1"

Test Layout





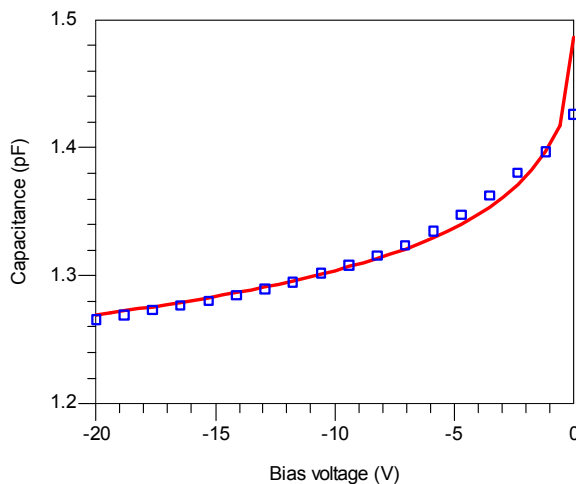
DC IV Characteristics



Legend: Solid Red lines-Model,
Blue \square Markers-Measured data

CV Characteristics

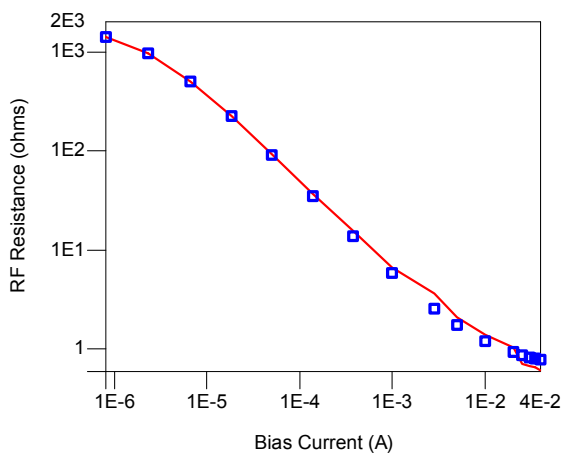
Simulated at 100 MHz



Legend: Solid Red lines-Model,
Blue \square Markers-Measured data

RI Characteristics

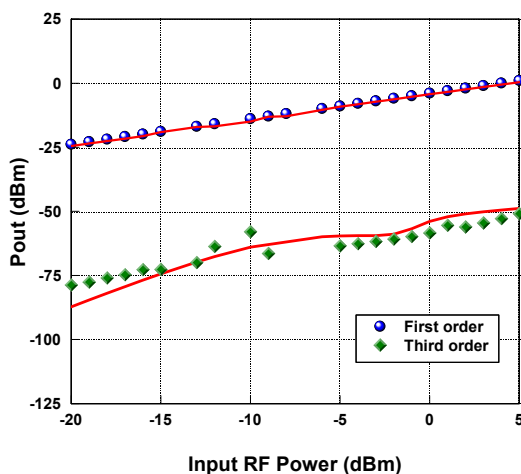
Simulated at 100 MHz



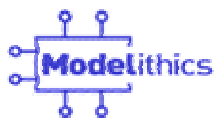
Legend: Solid Red lines-Model,
Blue \square Markers-Measured data

Harmonic Testing

Simulated at 1 GHz at zero-bias condition



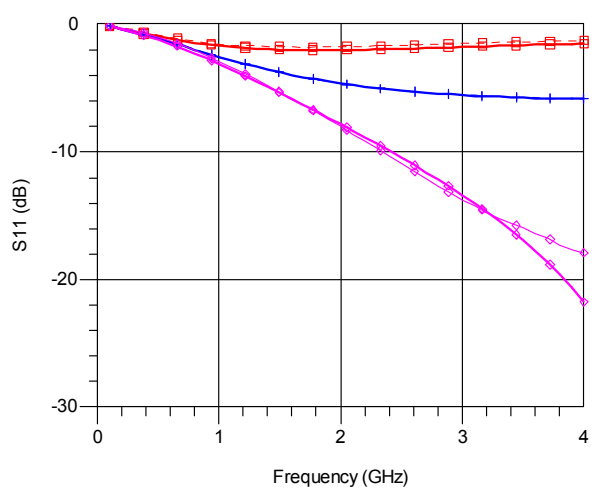
Legend: Solid Red lines-Model,
Markers-Measured data





S-Parameters

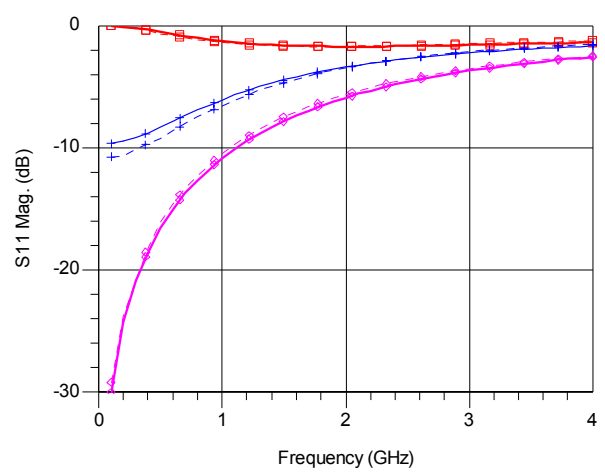
Simulated at 0.1V bias



Legend: □ 4mil Rogers 4350, + 14mil FR4,
◇ 59mil FR4
 Solid Line - model data,
 Dashed line - measured data,

S-Parameters

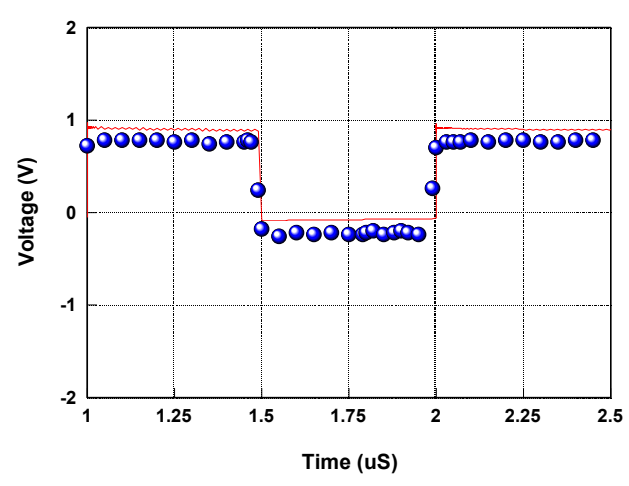
Simulated on 4 mil Rogers 4350 substrate



Legend: □ -20V, + 0.5V, ◇ 0.8V
 Solid line - model data,
 Dashed line - measured data

Time Domain Testing

Simulated at an input frequency of 1 MHz and an input amplitude of 1V. Bias condition is 0.6V



Legend: Solid Red lines-Model,
 markers-Measured data

